

**IN THE CLAIMS:**

Please substitute the following claims for the same-numbered claims in the application:

1. (Currently Amended) A simulator comprising:

a memory for storing a computer model of an integrated circuit comprising a device that is one of a transistor, a capacitor and a resistor and device having that has at least one performance attribute, wherein said computer model is generated based on a target model for said transistor and wherein said target model is created comprises using a target performance parameter for said performance attribute and is adapted to predict process and design variations of said device; and

a processor in communication with said memory device and adapted to execute said computer model,

wherein said target performance parameter includes a first bounded range and a second bounded range,

wherein said first bounded range comprises performance parameter variations within a single manufacturing process based on a single design for said device, and

wherein said second bounded range comprises performance parameter variations between multiple designs for said device.

2. (Currently Amended) The ~~computer model~~ simulator in claim 1, wherein said multiple designs are directed to variations of said single design.

3. (Currently Amended) The ~~computer-model~~ simulator in claim 1, wherein said target performance parameter is the same for a target model of said device and a final hardware design of said device.
4. (Currently Amended) The ~~computer-model~~ simulator in claim 1, wherein said target performance parameter is constrained within at least one of said first bounded range and said second bounded range.
5. (Currently Amended) The ~~computer-model~~ simulator in claim 4, wherein said target performance parameter is bounded by both of said first bounded range and said second bounded range.
6. (Currently Amended) The ~~computer-model~~ simulator in claim 4, wherein said multiple designs of said device are permitted to vary as long as said target performance parameter is maintained within said at least one of said first bounded range and said second bounded range.
7. (Currently Amended) The ~~computer-model~~ simulator in claim 1, wherein said target performance parameter comprises a plurality of performance points.
8. (Currently Amended) The ~~computer-model~~ simulator in claim 1, wherein said target performance parameter comprises at least a two-dimensional range of a plurality of performance points.

10/023,235

3

9. (Currently Amended) A computer-implemented method for designing a product having a device, wherein said device is one of a transistor, a capacitor and a resistor and a wherein said product is tolerant to variance in a given target performance parameter for a given performance attribute of said device, said method comprising:

designing said product device using a computer model that is based on a target model of said device, wherein said target model is created using said target performance parameter for said performance attribute,

wherein said target performance parameter includes a first bounded range and a second bounded range,

wherein said first bounded range comprises performance parameter variations within a single manufacturing process based on a single design for said device, and

wherein said second bounded range comprises performance parameter variations between multiple designs for said device.

10. (Previously Presented) The method of claim 9, wherein said multiple designs are directed to variations of said single design.

11. (Previously Presented) The method of claim 9, wherein said target performance parameter is the same for a target model of said device and a final hardware design of said device.

10/023,235

4

12. (Previously Presented) The method of claim 9, wherein said target performance parameter is constrained within at least one of said first bounded range and second bounded range.
13. (Currently Amended) The ~~computer-model~~ method in claim 9, wherein said multiple designs of said device are permitted to vary within said model as long as said target performance parameter remains within said first bounded range and said second bounded range.
14. (Currently Amended) A method of developing a product having a device with at least one performance attribute, wherein said device is one of a transistor, a capacitor and a resistor, said method comprising:
- providing design developing device goals for said device, wherein said device goals are based on product goals;
  - developing a target performance parameter for said performance attribute based on said device goals, wherein said target performance parameter includes a first bounded range and a second bounded range, wherein said first bounded range comprises performance parameter variations within a single manufacturing process based on a single design for said device, and wherein said second bounded range comprises performance parameter variations between multiple designs for said device;
  - producing a target model of said device based on said ~~design~~ device goals and said target performance parameter, wherein said target model is adapted to predict process and design variations of said device; and
  - ~~designing said device and said product with said device~~ based on said target model.

10/023,235

6

15. (Previously Presented) The method of claim 14, wherein said target performance parameter comprises a plurality of performance points.
16. (Previously Presented) The method of claim 15, wherein said multiple designs are directed to variations of said single design.
17. (Previously Presented) The method of claim 14, wherein said target performance parameter is the same for said target model of said device and a final hardware design of said device.
18. (Currently Amended) The ~~computer model~~ method in claim 14, wherein said multiple designs are permitted to vary as long as said target performance remains within said first bounded range and said second bounded range.
19. (Currently Amended) A method of designing a device with at least one performance attribute, wherein said device is one of a transistor, a capacitor and a resistor, said method comprising:
- providing a target model for said device;
  - wherein said target model is created based on a target performance parameter for said performance attribute,
  - wherein said target performance parameter includes a first bounded range and a second bounded range,

10/023,235

6

wherein said first bounded range comprises performance parameter variations within a single manufacturing process based on a single design for said device, and

wherein said second bounded range comprises performance parameter variations between multiple designs for said device;

developing a design for said device based on said target model;

proposing a modification of said design, wherein said modification comprises one of adding a particular feature into said design and modifying said particular feature already in said design;

determining primary parameters for said particular feature;

determining secondary parameters from said primary parameters; and

balancing design choices related to said modification and, particularly, to said primary parameters and said secondary parameters ~~so that said target performance parameter will remain~~ in order to maintain device performance within said first bounded range and said second bounded range of said target performance parameter.

20. (Original) The method of claim 19, wherein said step of determining secondary parameters further comprises the steps of:

determining at least one further secondary parameter from said secondary parameters;

and

correlating said secondary parameters to said at least one further secondary parameter.

21. (Original) The method of claim 19, further comprising the step of verifying that all primary and secondary parameters are within allowable limits.

10/023,235

7

22. (Original) The method of claim 19, wherein said primary parameters comprise first-order primary parameters and second-order primary parameters.
23. (Original) A method of designing a device, comprising the steps of:
- determining a set of design distributions that are within a given set of performance targets for a plurality of parameters;
  - altering different features of said design; and
  - determining whether said altered design is within said set of design distributions.
24. (Currently Amended) A method of developing a product having a device with at least one performance attribute, wherein said device is one of a transistor, a capacitor and a resistor, said method comprising:
- providing design developing device goals for said device, wherein said device goals are based on product goals for said product;
  - developing a target performance parameter for said performance attribute based on said device goals, wherein said target performance parameter includes a first bounded range and a second bounded range, wherein said first bounded range comprises performance parameter variations within a single manufacturing process based on a single design for said device, and wherein said second bounded range comprises performance parameter variations between multiple designs for said device;

producing a target model of said device based on said ~~design~~ device goals and said target performance parameter, wherein said target model is adapted to predict process and design variations of said device; and

~~simultaneously designing said device and~~ creating a computer model of said product, wherein said computer model of said product is based on said target model; and

simulating said computer model of said product to determine whether said product goals have been met.

25. (Previously Presented) The method of claim 24, further comprising:  
altering a device design to produce an altered device design; and  
accepting said altered device design only if said altered device design performs within said first bounded range and said second bounded range.
26. (Original) The method of claim 25, further comprising:  
refining said target model based on said altered device design; and  
designing at least said product based on said refined target model.
27. (Original) The method of claim 25, wherein said step of accepting said altered device design further comprises the steps of carrying out experiments on test chips.
28. (Original) The method of claim 24, wherein said step of designing said product further comprises:  
providing design goals for said product; and

developing a product model from said target model and from said design goals for said product.

29. (Original) The method of claim 28, further comprising:
- simulating said product model;
  - determining whether said design goals for said product have been met; and
  - altering said design of said product if said product design goals have been met.
30. (Currently Amended) The method of claim 24, wherein said accepting process comprises:
- calculating a primary parameter from a physical device feature;
  - ~~correlating a secondary parameter to said primary parameter;~~
  - calculating said a secondary parameter based on said primary parameter; and
  - comparing said secondary parameter to said target performance parameter.

31. (Original) The method of claim 30, further comprising correlating other secondary parameters from correlations to said secondary parameters.
32. (Original) The method of claim 30, wherein said primary parameter is directly related to said physical device feature.
33. (Previously Presented) The method of claim 30, wherein said calculating of said secondary parameter is performed using predetermined primary-to-secondary correlation calculations.
34. (Original) The method of claim 24, wherein said target performance parameters are the same for a target model of said device and a final hardware design of said device.
35. (Original) The method of claim 24, wherein device design is permitted to vary as long as said target performance parameters are maintained.
36. (Currently Amended) A program storage device readable by computer and tangibly embodying a model of an integrated circuit device that has at least one performance attribute, that is one of a transistor, a capacitor and a resistor, and that is executable by said computer. A  
~~computer medium storing a computer model of an integrated circuit device having at least one performance attribute, said model comprising:~~

10/023,235

11

a set of subroutines created using a target performance parameter for said performance attribute, wherein said set of subroutines, when executed by said computer, predict process and design variations of said device,

wherein said target performance parameter includes a first bounded range and a second bounded range,

wherein said first bounded range comprises performance parameter variations within a single manufacturing process based on a single design for said device, and

wherein said second bounded range comprises performance parameter variations between multiple designs for said device.

37. (Currently Amended) The ~~computer-medium~~ program storage device in claim 36, wherein said performance parameter is constrained within at least one of said first bounded range and said second bounded range.

38. (Currently Amended) The ~~computer-medium~~ program storage device in claim 36, wherein said performance parameter comprises a plurality of performance points.

39. (Currently Amended) The ~~computer-medium~~ program storage device, wherein said performance parameter comprises at least a two-dimensional range of a plurality of performance points.

40. (Currently Amended) A program storage device readable by computer and tangibly embodying a program of instructions executable by said computer to perform an integrated circuit development method, said method comprising A computer medium storing designs for an integrated circuit device having at least one performance attribute wherein said designs are generated utilizing a computer model, said model comprising:

producing a target model of a device for a product using a target performance parameter for a performance attribute of said device, wherein said device is one of a transistor, a capacitor and a resistor, and wherein said target model comprises a set of subroutines created using a target performance parameter for said performance attribute, that are adapted to predict process and design variations of said device,

wherein said target performance parameter includes a first bounded range and a second bounded range,

wherein said first bounded range comprises performance parameter variations within a single manufacturing process based on a single design for said device, and

wherein said second bounded range comprises performance parameter variations between multiple designs for said device; and

creating a computer model of said product, wherein said computer model of said product is based on said target model.